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High-performance passivated Black Silicon

KEYWORDS

- Black silicon
- Passivation
- Uniformity
- Scalable

Technology Market

Anti-reflective micro-structures for optical applications

- ✓ Light trapping for solar cells
- ✓ Optoelectronic applications
- ✓ Sensors

The UCL invention

Materials for optoelectronic applications and especially for the conversion of light into an electrical signal need to combine two main parameters: (i) to harvest a maximum number of photons out of an incident light and (ii) to recover a sufficient lifetime of the generated minority charge carriers.

In this framework, we developed black silicon (B-Si) structures having cutting-edge opto-electronical properties; such as an extremely low front reflectance **(R < 0.5%)**, thereby enhancing the light absorption (Fig. 1) in combination with a very high minority-carrier (MC) lifetime **(τ > 1ms** in the solar MCD range, Fig. 2). Such opto-electronic properties are of utmost importance for next-generation high-efficiency PERC and IBC solar cell technologies.

Additionally, the robust process proposed here is ***scalable*** on industrial size solar-graded wafers (15.6 cm x 15.6 cm) (inserts Fig.1). Moreover, the proposed innovation can replace the standard texturization step in PERC and IBC solar cell processing and is ***adaptable*** for both monocrystalline and polycrystalline silicon substrates (Fig. 3).

Key features of the invention

Properties

- ✓ Absorbance close to Yablonovitch limit
- ✓ Specular Reflectance < 0.5 %
- ✓ Hemispherical Reflectance < 2 %
- ✓ Angular reflectance (θ = 0° up to 60°) < 1%
- ✓ Minority-carrier lifetime > 1ms
- ✓ SRV < 5 cm/s for p/n-type, FZ, c-Si <100>
- ✓ Large scale homogeneity (243.36 cm^2)

Process

- ✓ Robust process for mono & poly-Si
- ✓ Single step Mask-free process
- ✓ Ultra-thin passivation layers
- ✓ Replacement of the KOH/TMAH steps
- ✓ Metal contamination-free plasma step
- ✓ Work on as-cut rough surfaces
- ✓ In-situ 2 µm surface silicon removal

Technology Status

TRL 4 – technology validated in lab

This work is the subject of an EP patent application filed on 20th March 2017 (application number EP17161813.5).

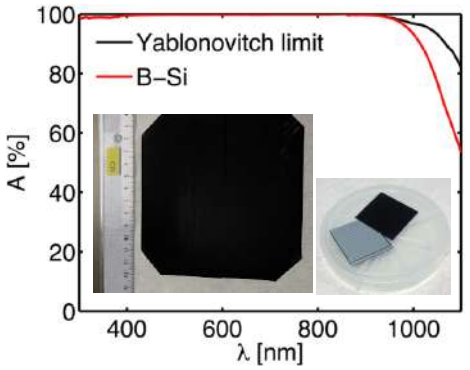

Fig. 1. Absorbance. Insert shows an Industry size solar wafer (left) and IBC solar cells (right) with our B-Si.

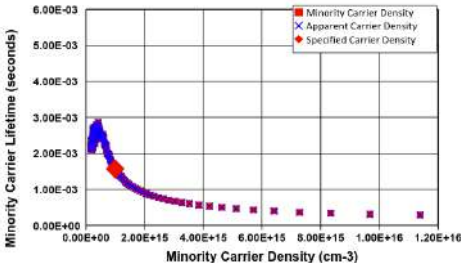

Fig. 2. MC-lifetime versus MCD measured using Sinton WCT-120 lifetime tester in transient photoconductance decay mode (zero instrument is performed prior to the measurements).

Fig. 3. Four wafers with B-Si (left). Comparison between two polycrystalline Si samples before and after B-Si step.

INTERESTED TO DEVELOP AND / OR COMMERCIALISE THIS TECHNOLOGY

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